

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 10 and 12 without prejudice and amend claims 1 and 4 as follows:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device, comprising:
 - a gate electrode formed on a substrate through a gate insulating film lying therebetween;
 - first and second diffused layers formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction type of the portion;
 - a wiring layer formed above the gate electrode;
 - a contact hole formed between the wiring layer and the substrate, said ~~contact~~ contact hole having a width which spans the gate electrode and the first diffused layer; [[and]]
 - a contact formed within the contact hole and electrically connecting the wiring layer to the first diffused layer and to the gate electrode,
 - another gate electrode formed on the substrate through another gate insulating film; and
 - a transistor for composing a semiconductor IC therein,
 - wherein the relative dielectric constant of the gate insulating film is higher than the one of said another gate insulating film.

2. (Original) A semiconductor device according to Claim 1, wherein the contact is connected also to the second diffused layer.

3. (Previously Presented) A semiconductor device according to Claim 1, comprising:

a third diffused layer formed on the substrate; and

an isolation area formed between the first and the third diffused layers, which separates the first and the third diffused layers from each other;

wherein the contact is connected further to the third diffused layer.

4. (Currently Amended) A semiconductor device, comprising:

a gate electrode formed on a substrate through a gate insulating film;

a diffused layer formed on the substrate;

a wiring layer formed above the gate electrode;

a contact hole formed between the wiring layer and the substrate, the contact hole having a width which spans the gate electrode and the diffused layer; [[and]]

a contact formed within the contact hole, electrically connecting the wiring layer to the diffused layer and to the gate electrode[.];

a source area and a drain area formed opposed to each other across the channel portion of the substrate existing under the gate electrode; and

a transistor for composing a semiconductor IC therein,

wherein the diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from

the first conduction type of the portion of the substrate; and a third portion that connects the first portion to the second portion, wherein the impurity concentration of the diffused layer is higher than the impurity concentration of the source area and the drain area.

5. (Original) A semiconductor device according to claim 4, wherein the contact is connected to the first portion and the second portion of the diffused layer.

6. (Previously Presented) A semiconductor device according to claim 4, comprising:

another diffused layer formed on the substrate; and

an isolation area formed between the diffused layer and said other diffused layer, which separates the diffused layer and the other diffused layer, wherein the contact is connected further to the other diffused layer.

7. (Previously Presented) A semiconductor device according to claim 1, comprising a SRAM cell, wherein the wiring layer is connected to a memory node of the SRAM cell.

8. (Original) A semiconductor device according to claim 1, comprising a bistable trigger circuit, wherein the wiring layer is connected to the memory node of the bistable trigger circuit.

9. (Original) A semiconductor device according to claim 1, comprising:
another gate electrode formed on the substrate through another gate insulating film,
and a transistor for composing a semiconductor integrated circuit therein, wherein
the film thickness of the gate insulating film is thinner than the one of the other gate
insulating film.

10. (Cancelled)

11. (Previously Presented) A semiconductor device according to claim 1,
comprising a source area and a drain area formed opposed to each other across a
channel portion of the substrate existing under the gate electrode, and a transistor
for composing a semiconductor IC therein, wherein the impurity concentrations of the
first diffused layer and the second diffused layer are higher than the ones of the
source and the drain areas.

12. (Cancelled)

13. (Previously Presented) A semiconductor device according to claim 4,
comprising a SRAM cell, wherein the wiring layer is connected to a memory node of
the SRAM cell.

14. (Original) A semiconductor device according to claim 4, comprising a
bistable trigger circuit, wherein the wiring layer is connected to the memory node of
the bistable trigger circuit.

15. (Original) A semiconductor device according to claim 4, comprising:
another gate electrode formed on the substrate through another gate insulating film,
and a transistor for composing a semiconductor integrated circuit therein, wherein
the film thickness of the gate insulating film is thinner than the one of the other gate
insulating film.

16. (Original) A semiconductor device according to claim 4, comprising
another gate electrode formed on the substrate through another gate insulating film,
and a transistor for composing a semiconductor IC therein, wherein the relative
dielectric constant of the gate insulating film is higher than the one of the other gate
insulating film.

17. (Cancelled)